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Total No. of Questions : 08] [Total No. of Pages : 02

M.Tech.

HARDWARE DESCRIPTION LANGUAGES

SUBJECT CODE :VL - 513

Paper ID : [E0723]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 50**

Instruction to Candidates:

1) Attempt any **Five** questions.
2) **All** questions carry equal marks.

Q1) (a) Compute A & not B or C nor 2 and D
where A = "110", B = "111", C = "011000" and D = "111011".

(b) Write a procedure to add two n-bit bit vectors in VHDL.

Q2) (a) Write VHDL structural model for a full subtractor using NAND gates.

(b) Write a function to convert bit vector to integer.

Q3) (a) Enumerate two predefined subtypes of type integer and declare them.

(b) Develop a functional model for a full adder using selected signal assignment statement.

(c) Write the order of precedence of VHDL operators. Name two unary operators.

Q4) (a) Write a declaration for vector a subtype of std_ulogic_vector, representing a byte. Declare a constant of this subtype, with each element having the value 'X'.

(b) Write the equivalent process for the selected signal assignment statement with bit_vector' (s,r) select

q < = unaffected when "00".
'0' when "01",
'1' when "10" | "1 1";

(c) Write an array type declaration for an array of 20 integers and a variable declaration for a variable of the type. Write a loop to calculate the average of the array elements.

Q5) (a) Write the three different forms of binding-indication and their syntax?

(b) Differentiate between functions and procedures?

(c) Why are configurations needed?

Q6) (a) Name two kinds of assignment statements that you can have in Verilog HDL model.

(b) What is the purpose of the timescale compiler directive? Give an example.

(c) Using the dataflow description style, write a Verilog HDL model for the exclusive or gate using AOI logic. Use the specified delays. For and gate 5 ns, or gate 4 ns, not gate 1 ns.

Q7) (a) Verilog HDL allows a net not to be explicitly declared. If so, how is the net kind determined?

(b) Identify the legal and illegal identifiers :

(i) COunT,
(ii) 1_2 Many,
(iii) **1,
(iv) Real?,
(v) \wait,
(vi) Initial.

(c) Write a system task to load a 32 by 64 word memory from a data file "memA.data"?

Q8) (a) When there are two or more assignments to the same target, how is the effective value for the target determined?

(b) Describe the behavior of a JK flip-flop using an always statement.