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Total No. of Questions : 09] [Total No. of Pages : 02

B.Tech. (Sem. - 4th)

DIGITAL ELECTRONICS

SUBJECT CODE : EC - 204

Paper ID : [A0307]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 x 2 = 20)*

a) Define bit, byte and nibble.

b) Find the complement of $A\overline{B}+\overline{B}C+C\overline{D}$.

c) What do you mean by weighted code? Give example.

d) Construct the truth table for $F=x\overline{y}+\overline{x}y$.

e) Draw the logic circuit for the expression $F=\overline{x}\,\overline{y}z+\overline{x}yz+x\overline{y}$.

f) Convert the given expression in canonical SOP form Y = AC + AB + BC.

g) What is universal shift register?

h) Give significance of priority encoder.

i) What is the difference between static and dynamic RAM?

j) Define noise margin. What is its importance?

Section - B

(4 x 5 = 20)

Q2) What are the applications of hexadecimal system?

Perform the following conversions:

(a) (225.225)10 into hexadecimal number.

(b) (10011.1101)2 into hexadecimal number.

Q3) What is the importance and applications of Gray code? Convert the binary number 10100111 to Gray code.

Q4) Implement the following function using 3 to 8 decoder

$f(A,B,C)=\sum m(0,1,4,5,7)$

Q5) What is the difference between level and edge triggering? Explain the working of master slave J-K flip flop.

Q6) Explain the working of R-2R ladder type D/A converter.

Section - C

(2 x 10 = 20)

Q7) (a) Design the circuit for one bit comparator.

(b) Design a full adder circuit using NAND gates only.

Q8) Design a synchronous decade counter to count in the following sequence

1, 0, 2, 3, 4, 8, 7, 6, 5

Q9) Draw the circuit of TTL NAND gate and explain its operation. Compare the TTL and ECL logic families.